REMARKS/ARGUMENTS

The present amendment is in response to the Office Action mailed October 6, 2003, in which Claims 13 through 19 are rejected, and claims 14 through 17 are objected to. Applicant has thoroughly reviewed the outstanding Office Action including the Examiner's remarks and the reference cited therein. The following remarks are believed to be fully responsive to the Office Action and, when coupled with the amendments made herein, are believed to render all claims at issue patentably distinguishable over the cited references.

Claims 1-12 are canceled due to pertain to non-elected claims. Claims 13 through 19 are amended herein. No claims are added. Accordingly, Claims 13 through 19 remains pending.

A new title is substituted for the original title for clearly indicating the invention to which the claims are directed. The original abstract is replaced by a new abstract attached in a new sheet. The whole specification is revised to correct all possible minor errors therein. It should be noted that all the corrections are made for clarification and are based on the application and drawings as originally filed. It is respectfully submitted that no new matter is added.

Applicant respectfully requests reconsideration in light of the above amendments and the following remarks.

CLAIMS REJECTIONS- 35 USC § 112, SECOND PARAGRAPH

With respect to first paragraph, page 4 of the Office Action, claims 14 to 17 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 14 to 17 are amended to more clearly and specifically recite the subject matter which applicant regards as the invention.

It is respectfully requests that the examiner's rejection of claims 14 to 17 under 35USC § 112, second paragraph be reconsidered and withdrawn.

CLAIMS REJECTIONS- 35 USC § 102(b)

With respect to second paragraph, page 5 of the Office Action, claims 13, 14 and 16 to 19 are rejected under 35 USC § 102(b) as being anticipated by Akagawa et al. (US Patent No. 5,960,308). Claim 13 is independent claim herein.

Applicant respectfully traverses this rejection on the grounds of the following reasons.

The present invention provides a wafer level package for producing chip size packages, as claimed in amended claim 13, which includes a plurality of chips on a surface of a wafer having trenches running through, each trench formed between the chips, and a filling material is filled in the trenches. Metal pads are formed on the surface

of the wafer. A photosensitive polymer layer is formed on the surface of the wafer and the metal pads are exposed. A first conductive layer is formed on the metal pads within the photosensitive polymer layer. A circuit distribution pattern is formed on the top of the photosensitive polymer layer and the first conductive layer. A protection layer is covered on the circuit distribution pattern and the photosensitive polymer layer, and a portion of the circuit distribution pattern is exposed. Conductive bumps are formed on the exposed circuit distribution pattern.

The wafer level package of the present invention can conduct testing before a cutting process. During the cutting process, the wafer is cut along the trenches filled with the filling material to separate each chip from the wafer, thus producing chip size packages.

As to the cited reference, Akagawa et al., which provides a chip size package, see FIG. 1 and col. 3, lines 63-67 and col. 4, lines 1-44. The chip size package of Akagawa et al. includes a chip 32, an Al pad 36 formed on the chip 32, a passivation film of silicon dioxide 34 formed on the surface of the chip 32 to make the Al pad 36 exposed, an insulation film of acrylic resin 38 formed on the passivation film of silicon dioxide 34, a via-hole 39 formed in the insulation film of acrylic resin 38 and the passivation film of silicon dioxide 34 to expose the Al pad 36, a circuit pattern (40,41,43) formed on the insulation film of acrylic resin 38 and electrically connected with the Al pad 36, an electro-insulation layer 42

formed on the insulation film of acrylic resin 38 and the circuit pattern (40,41,43) , a via-hole 44 formed in the electro-insulation layer 42 to expose a portion 43 of the circuit pattern, a conductive bump 46 formed in the via-hole 44 and electrically connected with the exposed portion 43 of the circuit pattern, a resist resin protective sheet 48 covering the side walls of the chip 32, the passivation film 34 and the insulation film 38 for the purpose of inhibiting moisture invasion through the boundaries between the respective layers.

The present invention provides a wafer level package as claimed in claim 13. However, Akagawa et al. provides a chip size package. Both of the two are different. Moreover, in Akagawa et al., the resist resin protective sheet 48 covering the side walls of the chip 32, the passivation film 34 and the insulation film 38 is used for the purpose of inhibiting moisture invasion through the boundaries between the respective layers. The resist resin protective sheet 48 is totally different from the trench structure with the filling material as claimed in the amended claim 13 of the present invention. Therefore, Akagawa et al. neither teaches nor suggests the trench structure with the filling material as claimed in the amended claim 13 of the present invention to facilitate to conduct the testing of the wafer level package before the cutting process and then cut each chip size package along the trenches of the wafer. In other words, Akagawa et al. provides a chip size package that needs to be previously

cut from a wafer before the testing process. Thus, the wafer level package as claimed in the amended claim 13 can not be anticipated by Akagawa et al. The amended claim 13 of the present invention is patentably distinguished over the cited reference, Akagawa et al.

Claims 14, 16 to 19 depend upon the amended claim 13, each of which including all limitations thereof. Therefore, claims 14, 16 to 19 also can not be anticipated by Akagawa et al. Claims 14, 16 to 19 are patentably distinguished over the cited reference, Akagawa et al.

Accordingly, Applicant respectfully requests that the examiner's rejection of claims 13, 14 and 16 to 19 under 35USC § 102(b) be reconsidered and withdrawn.

CLAIMS REJECTIONS- 35 USC § 102(e)

With respect to second paragraph, page 6 of the Office Action, claims 13, 14 and 16 to 19 are rejected under 35 USC § 102(e) as being anticipated by Chakravorty (US Patent No. 6,181,569B1).

Applicant respectfully traverses this rejection.

The cited reference, Chakravorty provides a chip size package, see FIG. 6 and col. 7, lines 45 to 55, col. 8, lines 1-61 and col. 12, lines 34-40. The chip size package includes a chip 302, a plurality of pads 303 formed on the chip 302, a first dielectric layer 305 formed on the chip 302, a plurality of via-holes 306 formed on the first dielectric layer 305 to expose the pads 303, a circuit pattern 307 formed on the first dielectric

layer 305 and electrically connected with the pads 303, a second dielectric layer 308 formed on the first dielectric layer 305 and the circuit pattern 307, a plurality of via-holes 309 formed on the second dielectric layer 308 to expose a portion of the circuit pattern 307, a metallic layer 310 formed on the via-hole 309 in the second dielectric layer 308 and electrically connected with the exposed portion of the circuit pattern 307, a plurality of conductive bumps 311 formed on the metallic layer 310. See FIG. 9a of Chakravorty, the wafer 301 shows scribe lines 316 thereon along which the wafer 301 is sawed to sections 317. Each section 317 includes numerous chips.

The present invention provides a wafer level package as claimed in claim 13. However, Chakravorty provides a chip size package. Both of the two are different. Moreover, as mentioned above, the scribe lines 316 shown on the wafer 301 in FIG. 9a of Chakravorty are different from the trench structure with the filling material as claimed in the amended claim 13 of the present invention. Chakravorty neither teaches nor suggests the trench structure with the filling material as claimed in the amended claim 13 of the present invention to facilitate to conduct the testing of the wafer level package before the cutting process and then cut each chip size package along the trenches of the wafer. In other words, Chakravorty provides a chip size package that needs to be previously cut from a wafer before the testing process. Thus, the wafer level package as claimed in the amended claim 13 can not be anticipated by Chakravorty.

The amended claim 13 of the present invention is patentably distinguished over the cited reference, Chakravorty.

Claims 14, 16 to 19 depend upon the amended claim 13, each of which including all limitations thereof. Therefore, claims 14, 16 to 19 also can not be anticipated by Chakravorty. Claims 14, 16 to 19 are patentably distinguished over the cited reference, Chakravorty.

Accordingly, Applicant respectfully requests that the examiner's rejection of claims 13, 14 and 16 to 19 under 35USC § 102(e) be reconsidered and withdrawn.

CLAIMS REJECTIONS- 35 USC § 103(a)

With respect to second paragraph, page 7 of the Office Action, claim 15 is rejected under 35 USC § 103(a) as being unpatentable over Akagawa et al. (US Patent No. 5,960,308) in view of Ishida (US Patent No. 5,686,702).

Applicant respectfully traverses this rejection.

Claim 15 depends upon claim 13, including all limitations thereof.

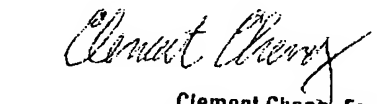
The cited reference, Ishida teaches using polyimide as the material of multiple dielectric layers on a substrate, see FIG. 1, col. 4, lines 15-16. It is apparent that Akagawa et al. and Ishida fail to teach or suggest the recitation of the claim 15 that the trench structure with the filling material, whether standing alone or in combination. Hence, claim 15 is patentably distinguished over the two references.

Accordingly, Applicant respectfully requests that the examiner's 35USC103(a) rejection of claim 15 be reconsidered and withdrawn.

CONCLUSION

In light of the above remarks, Applicant respectfully submits that all pending claims 13 through 19 as currently presented are in condition for allowance. Favorable reconsideration is respectfully requested.

Respectfully submitted,



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